forming a control electrode of a polysilicon layer on first and second regions. The step of forming a control electrode includes a step of introducing an impurity into the polysilicon layer within the first region at a relatively low dose. The step of forming a control electrode further includes a subsequent step of introducing the impurity into the polysilicon layer within the second region at a relatively high dose. This subsequent step includes introducing nitrogen into a lower portion of the polysilicon layer within the second region. Applicants respectfully traverse this rejection, as a *prima facie* case of obviousness under 35 U.S.C. §103(a) has not been established.

To establish a *prima facie* case of obviousness under 35 U.S.C. §103, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation in the references themselves to modify the reference or to combine reference teachings. Third, there must be reasonable expectation of success for the modification or combination of references. Further, the teaching or suggestion to make the modification or combination of prior art and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *In re Vaeck*, 947 F.2d 488,20 USPQ2d 1438 (Fed. Cir. 1991). Additionally, there must be particular finding as to the specific understanding or principle within the knowledge of a skilled artisan that would have motivated one with no knowledge to the claimed invention to combine or modify references. *In re Kotzab*, 217 F.3d 1365, 55 U.S.P.Q.2d 1313 (Fed. Cir. 2000). Also, see M.P.E.P. §2143.

Japanese Patent Publication No. 04157766 relates to the manufacture of a silicon gate p-channel MOSFET. This reference discloses a selective oxide film 3 and a gate oxide film 4 formed on substrate 1. A polyside film 7, made of p-type polysilicon film 5 and a tungsten silicide film 6, is formed. A n-channel MOSFET is masked with resist film 8. Nitrogen ions

are then implanted into the p-channel MOSFET. Unlike the requirements of claims 14 and 15, Japanese Patent Publication No. 04157766 does not disclose introducing an impurity into a polysilicon layer within a first region at a relatively low dose and within a second active region at a relatively high dose. Japanese Patent Publication No. 04157788 also does not disclose introducing nitrogen into the second regions that contains a relatively high dose of impurity, as required by claims 14 and 15. Accordingly, this reference is deficient in teaching or suggesting all the limitations required by claims 14 and 15.

Choi relates to a selective diffusion process for forming both n-type and p-type gates with a single masking step. The Office Action cites Figures 3A - 3C and the specification in column 8, line 16-18. Figures 3A - 3C illustrates the formation of p-channel devices with p-type and n-type polysilicon gates and n-channel devices with n-type and p-type polysilicon gates. The disclosed polysilicon layer 200 is rendered to be p-type conductive by a blanket implant or by diffusion. It is further disclosed that the polysilicon layer 200 is divided into four portions (200a-200d). It is disclosed that portions 200a and 200b are counter-doped to be n-type conductive. This disclosure does not alleviate the above-mentioned deficiencies of Japanese Patent Publication No. 04157766. This is evident and apparent, as the disclosure of Choi does not teach or suggest introducing an impurity in first and second active regions, wherein impurity is a relatively low dose within the first region and a relatively high dose within the second region. There is no disclosure in Figures 3A-3C or the accompanying description in column 5 of an impurity with different concentrations in the respective first and second active regions. As portions 200a and 200b are disclosed as being counter-doped, these portions inherently do not have the same impurity as portions 200c and 200d in a different concentration. Further, the disclosure in Choi does not alleviate the deficiency of nitrogen being introduced into the claimed second region.

Gardner et al. relates to a method of making an asymmetrical IGFET with a silicide contact on the drain without a silicide contact on the source. The Office Action cites column 10, lines 19-26 and column 12, lines 1-11. The Office Action asserts that "Gardner et al. discloses the dependence of threshold voltage on concentration of dopant in the gate of a MOSFET and the formation of MOSFET's having different concentrations of dopant on the same wafer..." The Applicants respectfully traverse this assertion, as Gardner et al. merely discloses a single n-channel device. Gardner et al. discloses in column 10, lines 16-26 that a photoresist layer is provided over IGFET that can cover substantially all of the gate, substantially none of the gate, or various amounts in between. It is disclosed that the photoresist layer can be used to adjust the threshold voltage of the gate. However, this disclosure does not accommodate for the introduction of impurity in a first active region at a relatively low dose and then a second active region at a relatively high dose. This is apparent because as in claims 14 and 15 the first and second regions are defined by a field oxide film which is not suggested in Gardner et al. Gardner et al. merely suggests a single active region. Accordingly, Gardner et al. does not alleviate the deficiencies of Japanese Patent Publication No. 04157766 or Choi.

Chou et al. does not disclose a step of introducing an impurity within a first active region in a relatively low dose and introducing the impurity into a second region at a relatively high dose, as required by claims 14 and 15. Further, this reference does not teach or suggest introduction nitrogen in the claimed second region. Accordingly, Choi et al. does not alleviate the above-mentioned deficiencies of Japanese Publication Patent No. 04157766, Choi, or Gardner et al.

Kuroi et al. relates to the impact of nitrogen implantation into a highly doped polysilicon gate. The Office Action states that Kuroi et al. discloses the effects of different

nitrogen concentrations and dope concentrations in the gate of a MOSFET and cites Figures 2 and 3. However, Figures 2 and 3 and the accompanying disclosure on page 772 does not disclose any aspect to dopant concentrations in the gate of a MOSFET. Further, this disclosure does not teach or suggest introducing an impurity into the polysilicon layer within a first region and a second region, wherein the impurity in the first region is at a relatively low dose and the impurity in the second region is at a relatively high dose. Accordingly, the disclosure of Kuroi et al. does not alleviate the above-mentioned deficiencies of either Japanese Patent Publication No. 04157766, Choi, Gardner et al., or Chou et al.

A *prima facie* case of obviousness has not been established. The cited prior art references, alone or in combination, do not teach or suggest all of the requirements of claims 14 and 15. This is evident and apparent, as none of the cited prior art references disclose, teach, or suggest introducing an impurity into a polysilicon layer within a first region and second region, wherein the impurity in the first region is at a relatively low dose and the impurity in the second region is at a relatively high dose. Further, none of the cited prior art references, alone or in combination, disclose, teach, or suggest the introduction of nitrogen in the claimed second region. At least for these reasons, the Applicants respectfully request that the rejection of claims 14 and 15 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

Claims 16-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Japanese Patent Publication No. 04157766, Gardner et al., Choi, Chou et al., and Kuroi et al. These claims require a method of manufacturing a semiconductor device. The method comprises a step of forming a control electrode, which includes an impurity and nitrogen, in each of a first and second transistor. The method comprises a subsequent step of masking the first transistor. The method further comprises a

subsequent step of introducing nitrogen into the control electrode of only the second transistor. This rejection is respectfully traversed, as a *prima facie* case of obviousness has not been established. The requirements for establishing a *prima facie* case of obviousness, a description of Japanese Patent Publication No. 04157766, Gardner et al., Choi, Chou et al., and Kuroi et al. have been set forth above.

Japanese Patent Publication No. 04157766 is unlike claims 16-18, as there is no disclosure of forming a control electrode which includes an impurity and nitrogen in each of the first and second transistors. Accordingly, this reference is deficient in teaching or suggesting all of the claimed limitations required by claim 16-18.

Gardner et al. does not alleviate the above-mentioned deficiencies of Japanese Patent Publication No. 04157766. This is evident and apparent, as Gardner et al. does not disclose a method comprising a step of masking a first transistor and a subsequent step of introducing nitrogen into the gate electrode of only a second transistor. Further, Gardner et al. merely relates to a single transistor.

Neither Choi, Chou et al., nor Kuroi et al. alleviate the above-mentioned deficiencies of Japanese Patent Publication No. 04157766 or Gardner et al. This is evident and apparent, as these references contain no disclosure of forming a control electrode, which include an impurity and nitrogen in each of a first and second transistor, wherein the first transistor is masked and nitrogen is introduced into the control electrode of only the second transistor.

A *prima facie* case of obviousness has not been established in rejection of claims 16-18 under 35 U.S.C. §103(a) for at least a couple of reasons. First, the cited prior art references, alone or in combination, do not disclose, teach, or suggest all of the limitations required by claims 16-18. Second, the cited prior art references lack the requisite particular motivation to be combined to teach or suggest all the limitations required by claims 16-18.

Accordingly, the Applicants respectfully request reconsideration and withdrawal of the rejection of claims 16-18 under 35 U.S.C. §103(a).

Claims 19-27 are rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Japanese Patent Publication No. 04157766, Gardner et al., Choi , Chou et al., and Kuroi et al. These claims require a method comprising a step of forming first and second control electrodes on a gate insulation film of a first and second transistors. The first control electrode includes an impurity of a second conductivity type and nitrogen of a first concentration. The second control electrode includes nitrogen of a second concentration different from the first concentration. The Applicants respectfully traverse this rejection, as a *prima facie* case of obviousness has not been established. The requirements for establishing a *prima facie* case of obviousness and a description of the cited prior art references have been discussed above.

Japanese Patent Publication No. 04157766 does not teach or suggest all of the requirement of claims 19-27. This is an evident and apparent, as the disclosure does not teach or suggest a first control electrode including nitrogen of a first concentration and a second control electrode including nitrogen of a second concentration. Neither Choi, Kuroi et al., Gardner et al. nor Chou et al. alleviate this deficiency of Japanese Patent Publication No. 04157766.

A *prima facie* case of obviousness has not been established for at least because the cited prior art references, alone or combination, do not teach or suggest all of the limitations set forth in claims 19-27. At least for this reason, the Applicants respectfully request that the rejection of claims 19-27 under 35 U.S.C.§103(a) be reconsider and withdrawn.

In the rejections of claims 14-27 under 35 U.S.C. §103(a), Official Notice was taken that "formation of a capacitor connected to a source/drain region of a MOSFET

was known at the time of Applicant's invention and formation of DRAM's. It would have been within the scope of ordinary skill in the art to combine the known process with that made obvious by the combination of references discussed above to enable DRAM formation."

Official Notice may be taken of facts outside of the record which are capable of instant and unquestionable demonstration as being "well-know" in the art. *In re Ahlert*, 424 F.2d 10888, 1091, 165 USPQ 418, 420 (CCPA 1970). As set forth in M.P.E.P. §2144.03, if an applicant traverses an assertion made by Official Notice, a reference should be cited in support of this assertion. The Applicants are unable to instantly and questionably confirmed asserted facts made by Official Notice. In accordance with M.P.E.P. §2144.03, the Applicants respectfully traverse this taking of Official Notice.

In view of the above, it is believed that this application is in condition for allowance, such a notice is respectfully solicited. If there are any questions regarding this amendment or the application in general, a telephone call to the undersigned would be appreciated.

Respectfully submitted,

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